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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Question Set-6 Digital Technologies and Microprocessor

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A. Objectives Questions:

1. The universal logic gate is ……
   a) AND gate
   b) OR gate
   c) NAND gate
   d) NOT gate
2. In PUSH instruction, after each execution of the instruction, the stack pointer is
   a) incremented by 1
   b) decremented by 1
   c) incremented by 2
   d) decremented by 2
3. The instructions that are used for reading an input port and writing an output port respectively are
   a) MOV, XCHG
   b) MOV, IN
   c) IN, MOV
   d) IN, OUT
4. The instruction that loads the AH register with the lower byte of the flag register is
   a) SAHF
   b) AH
   c) LAHF
   d) PUSHF
5. The instruction that supports addition when carry exists is
   a) ADD
   b) ADC
   c) ADD & ADC
   d) None of the mentioned
6. Example of an external interrupt is
   a) divide by zero interrupt
   b) keyboard interrupt
   c) overflow interrupt
   d) type2 interrupt
7. During the execution of an interrupt, the data pushed into the stack is the content of
   a) IP
   b) CS
   c) PSW
   d) All of the mentioned

8. The step included in generating delays is
   a) determining exact required delay
   b) selecting instructions for delay loop
   c) finding period of clock frequency
   d) all of the mentioned
9. An interrupt breaks the execution of instructions and diverts its execution to
   a) Interrupt service routine
   b) Counter word register
   c) Execution unit
   d) control unit
10. The feature of mode 2 of 8255 is
   a) single 8-bit port is available
   b) both inputs and outputs are latched
   c) port C is used for generating handshake signals
   d) all of the mentioned

B. Short Answer Types Questions:

1. What is the need for ALE signal in 8085 microprocessor?
2. List the five interrupt pins available in 8085.
3. Differentiate Software and Hardware interrupts
4. What is mean by TRAP interrupt and its significance?
5. What is the need for interfacing?
6. Compare memory mapped I/O and peripheral mapped I/O
7. What is interrupt?.
8. Name the vectored and non vectored interrupt of 8085 system.
9. What is the need for a timing diagram?
10. Define (i) Instruction cycle (ii) Machine cycle

C. Long Answer Types Questions:

1. Write in brief about the internal architecture of microprocessor 8085.
2. Draw the timing diagram of OPCODE FETCH machine cycle.
3. Explain the functions of 8085 signals.
4. Design a microprocessor system to interface an 8K × 8 EPROM and 8K × 8 RAM
5. Write an ALP for Addition of two 16 bit numbers using 8086.

Solutions:

A. Objectives Questions:

1. Answer: c
   Explanation: NAND logic gate is the universal logic gate.
2. Answer: d
   Explanation: The actual current stack-top is always occupied by the previously pushed data. So, the push operation decrements SP by 2 and then stores the two bytes contents of the operand onto the stack.
3. Answer: d
   Explanation: The address of the input/output port may be specified directly or indirectly.
   Example for input port: IN AX, DX; This instruction reads data from a 16-bit port whose address is in DX and stores it in AX
   Example for output port: OUT 03H, AL; This sends data available in AL to a port whose address is 03H.
4. Answer: c
   Explanation: The instruction LAHF(Load AH from a lower byte of Flag) may be used to observe the status of all the condition code flags(except overflow flag) at a time.
5. Answer: b
   Explanation: ADC(Add with Carry) instruction performs the same operation as ADD operation, but adds the carry flag bit to the result.
6. Answer: b
   Explanation: Since the keyboard is external to the processor, it is an external interrupt.
7. Answer: d
   Explanation: The contents of IP, CS and PSW are pushed into the stack during the execution.
8. Answer: d
   Explanation: The delays can be generated step wise.
9. Answer: a
   Explanation: An interrupt transfers the control to interrupt service routine (ISR). After executing ISR, the control is transferred back again to the main program.
10. Answer: d
    Explanation: In mode 2 of 8255, a single 8-bit port is available i.e group A.

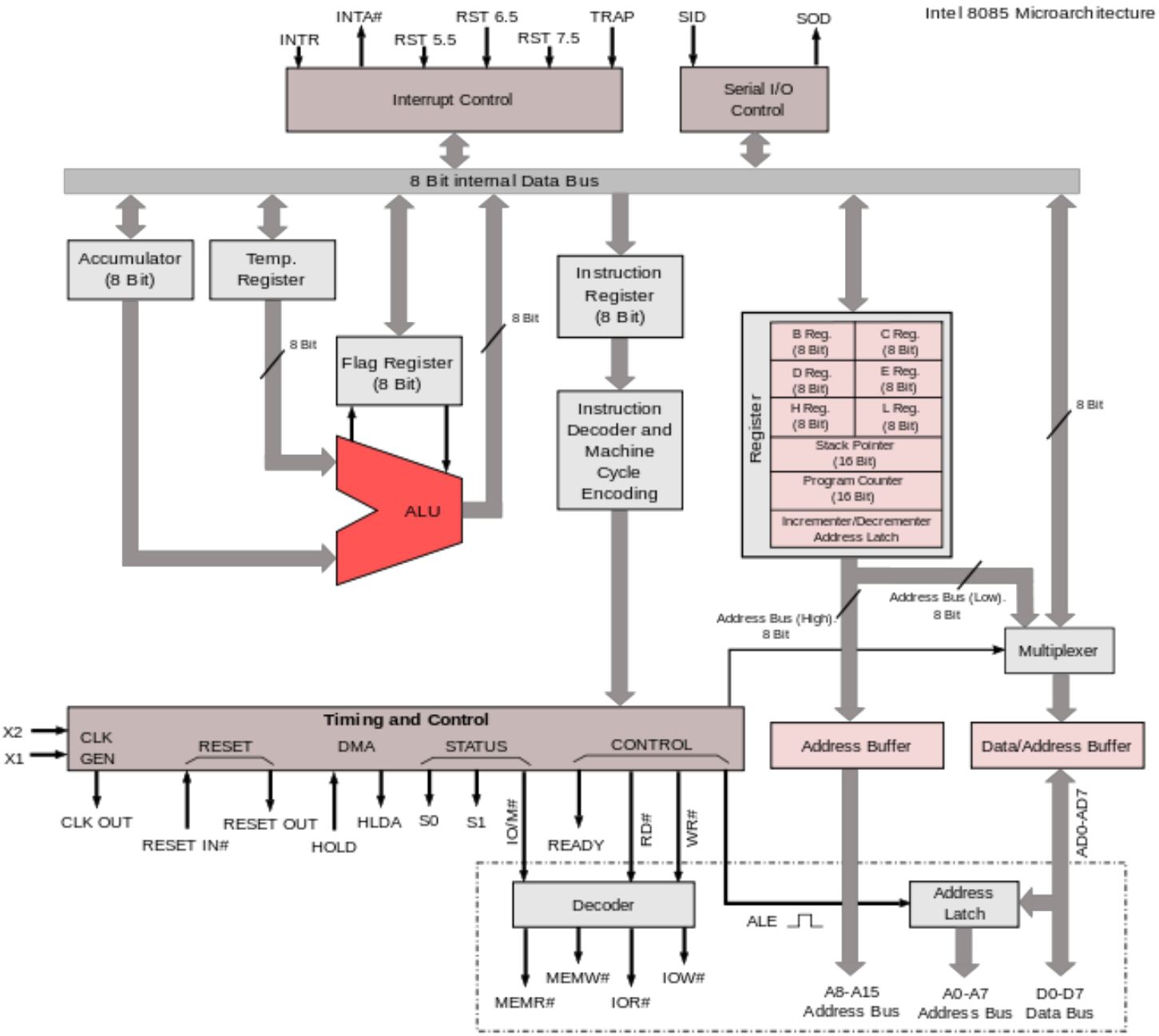
B. Short Answer Types Questions

1. The ALE signal goes high at the beginning of each machine cycle indicating the availability of the address on the address bus, and the signal is used to latch the low order address bus.
2. Interrupt pins are:
   INTR, TRAP, RST 7.5, RST 6.5, RST 5.5
3. The Software interrupt is initiated by the main program, but the hardware interrupt is initiated by the external device. In 8085, Software interrupts cannot be masked or disabled, but in hardware interrupts except TRAP all other interrupts can be masked. In 8086, Software interrupts cannot be masked or disabled, but in hardware interrupts except NMI all other interrupts can be masked.
4. TRAP is a Non maskable interrupt of 8085. It is not disabled by processor reset or after recognition of the interrupt.
5. Generally I/O devices are slow devices. Therefore the speed of I/O devices does not match with the speed of microprocessor. And so an interface is provided between system bus and I/O devices.
6. **Memory Mapped I/O:** 16-bit device address, data transfer between any general-purpose register and I/O port. The memory map (64K) is shared between I/O device and system memory. More hardware is
   required to decode 16-bit address Arithmetic or logic operation can be directly performed with I/O data.
   Peripheral Mapped I/O: 8-bit device address, Data is transfer only between accumulator and I.O port, The I/O map is independent of the memory map; 256 input device and 256. Output device can be connected Less hardware is required to decode 8-bit address, Arithmetic or logical operation cannot be directly performed with I/O data.
7. Interrupt is a signal send by an external device to the processor so as to request the processor to perform a particular task or work
8. When an interrupt is accepted, if the processor control branches to a specific address defined
   by the manufacturer then the interrupt is called vectored interrupt. In Non-vectored interrupt there is no specific address for storing the interrupt service routine. Hence the interrupted device should give the address of the interrupt service routine.
9. The timing diagram provides information regarding the status of various signals, when a machine cycle is executed. The knowledge of timing diagram is essential for system designer to
   select matched peripheral devices like memories, latches, ports, etc, to form a microprocessor system.
10. i) The sequence of operations that a processor has to carry out while executing the
    instruction is called Instruction cycle. Each instruction cycle of a processor indium consists of a number of machine cycles.
    (ii) The processor cycle or machine cycle is the basic operation performed by the processor. To execute an instruction, the processor will run one or more machine cycles

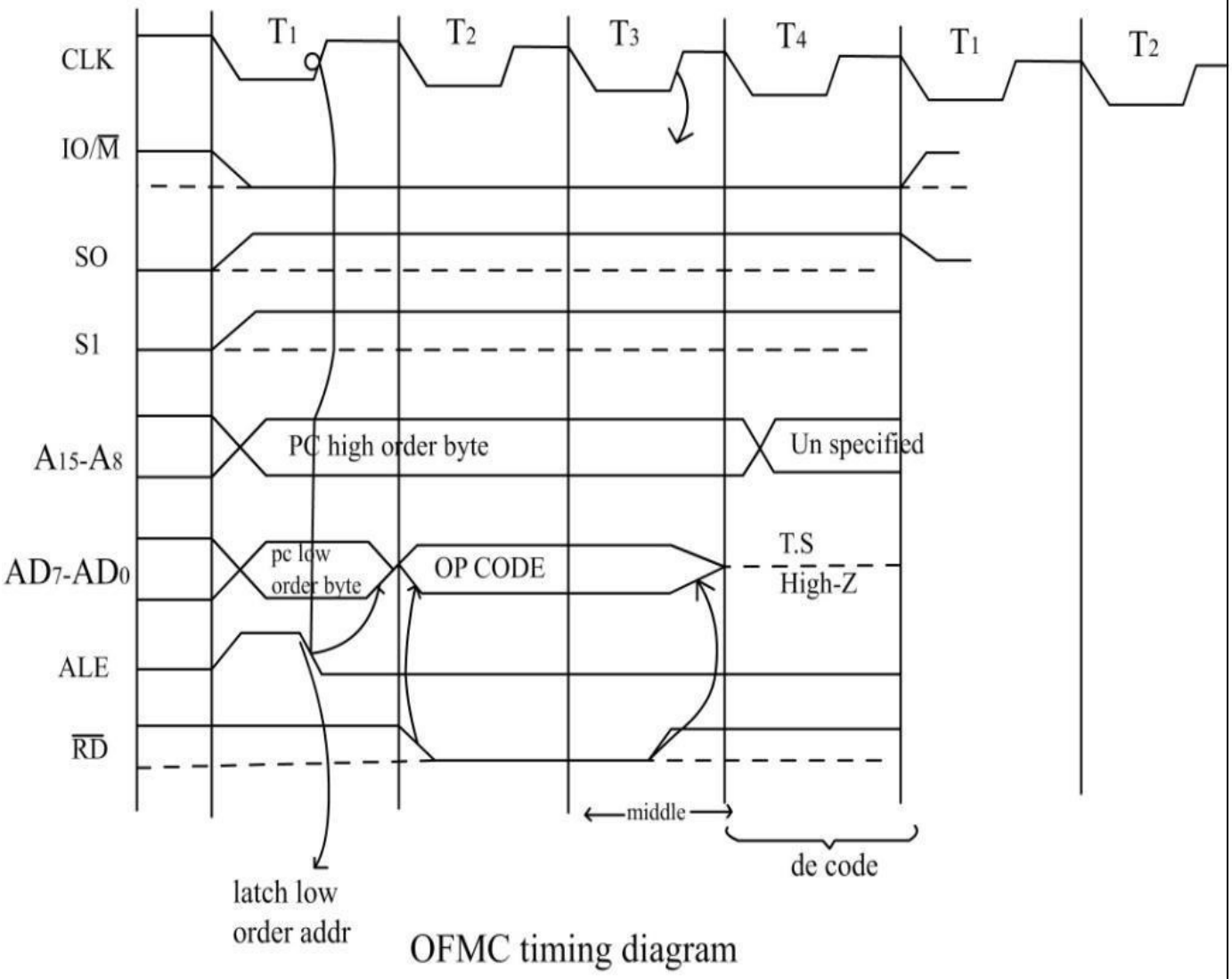
in a particular order. Opcode fetch, memory read, memory write, I/O read, I/O write, interrupt acknowledge, halt, hold and reset.

C. Long Answer Types Questions:

1. Internal architecture of microprocessor 8085

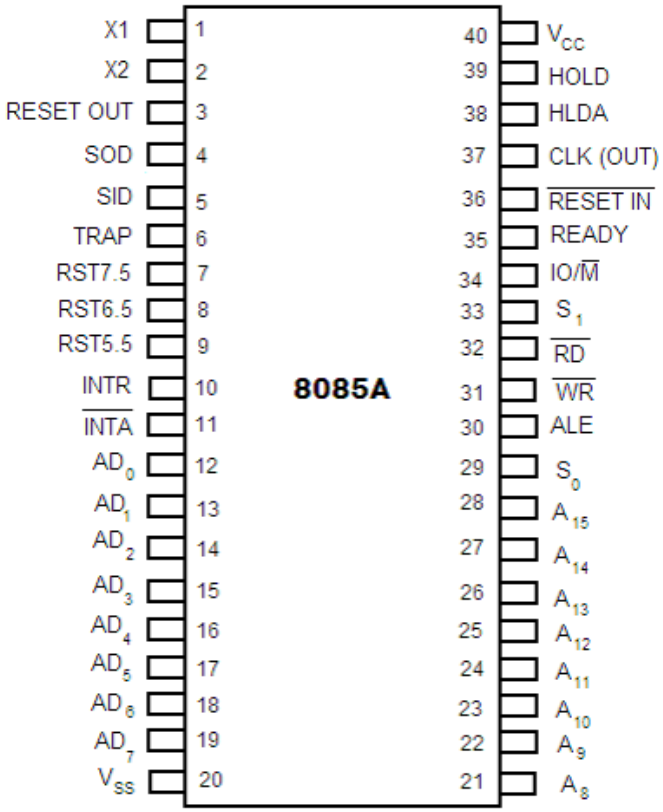


2. OPCODE FETCH machine cycle



OFMC timing diagram

3. Pin Diagram and Pin description of 8085



8085 is a 40 pin IC, The signals from the pins can be grouped as follows

- Power supply and clock signals
- Address bus
- Data bus
- Control and status signals
- Interrupts and externally initiated signals
- Serial I/O ports

Power supply and Clock frequency signals:

Vcc: + 5 volt power supply

Vss: Ground

X1, X2 : Crystal or R/C network or LC network connections to set the frequency of internal clock generator. The frequency is internally divided by two. Since the basic operating timing frequency is 3 MHz, a

6 MHz crystal is connected externally. CLK (output)-Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

Address Bus:

A8 - A15: (output; 3-state)

It carries the most significant 8 bits of the memory address or the 8 bits of the I/O address.

Data bus:

AD0 - AD7 (input/output; 3-state)

These multiplexed set of lines used to carry the lower order 8 bit address as well as data bus.

- During the opcode fetch operation, in the first clock cycle, the lines deliver the lower order address A0 - A7. •In the subsequent IO / memory, read / write clock cycle the lines are used as data bus.
- The CPU may read or write out data through these lines.

Control and Status signals:

ALE (output) - Address Latch Enable.

- It is an output signal used to give information of AD0-AD7 contents.
- It is a positive going pulse generated when a new operation is started by uP.
- When pulse goes high it indicates that AD0-AD7 are address.
- When it is low it indicates that the contents are data.

RD (output 3-state, active low)

- Read memory or IO device.
- This indicates that the selected memory location or I/O device is to be read and that the data bus is ready for accepting data from the memory or I/O device

WR (output 3-state, active low)

- Write memory or IO device.
- This indicates that the data on the data bus is to be written into the selected memory location or I/O Devices.

IO/M (output) - Select memory or an IO device.

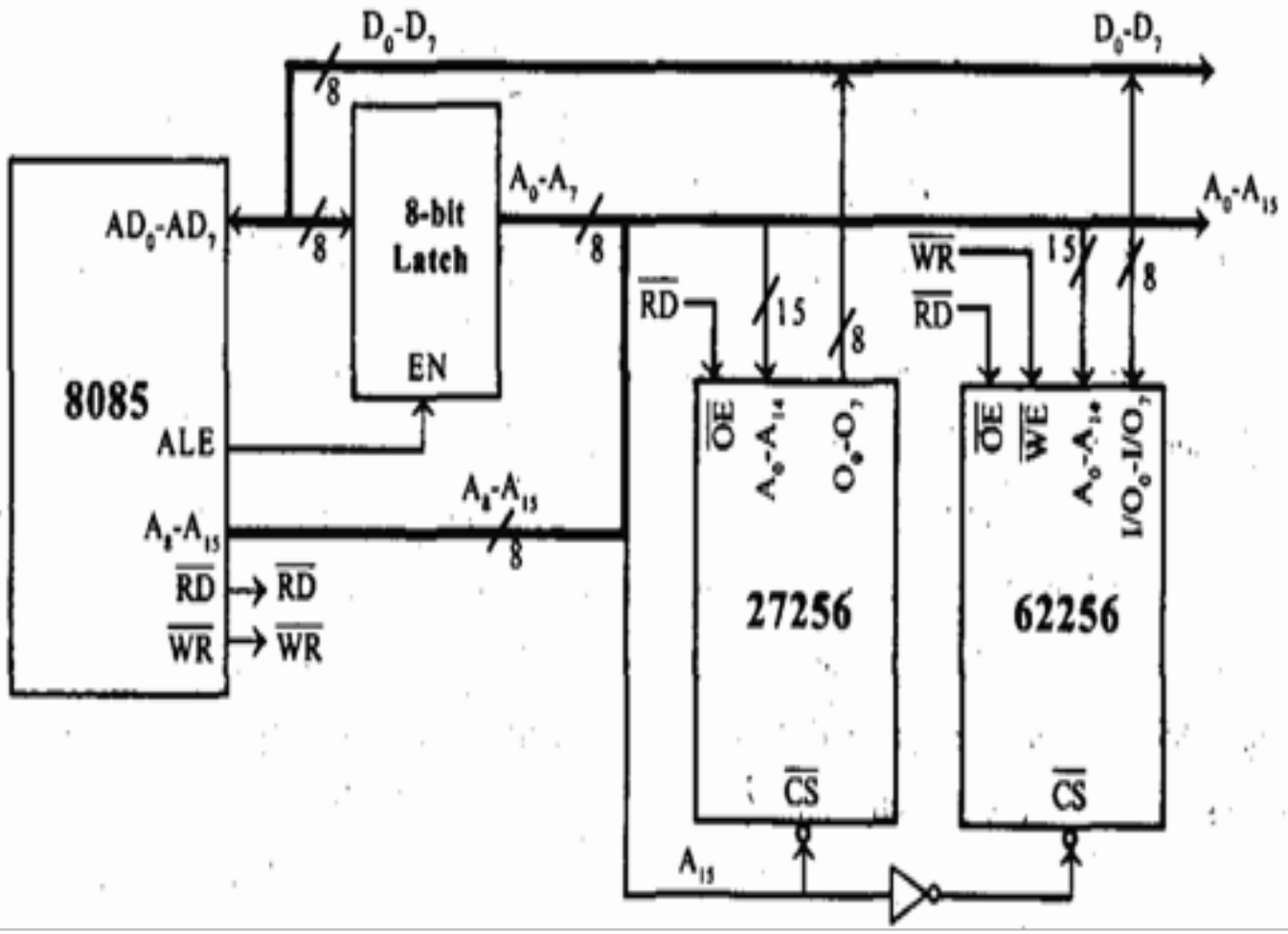
This status signal indicates that the read / write operation relates to whether the memory or I/O device.

It goes high to indicate an I/O operation.

It goes low for memory operations

4. Consider a system in which the available 64kb memory space is equally divided between EPROM and RAM. Interface the EPROM and RAM with 8085 processor.

- Implement 32kb memory capacity of EPROM using single IC 27256.
- 32kb RAM capacity is implemented using single IC 62256.
- The 32kb memory requires 15 address lines and so the address lines A0 - A14 of the processor are connected to 15 address pins of both EPROM and RAM.
- The unused address line A15 is used as to chip select. If A15 is 1, it select RAM and If A15 is 0, it select EPROM.
- Inverter is used for selecting the memory.
- The memory used is both Ram and EPROM, so the low RD and WR pins of processor are connected to low WE and OE pins of memory respectively.
- The address range of EPROM will be 0000H to 7FFFH and that of RAM will be 7FFFH to FFFFH. Two sets of above procedure is used for 64kb of EPROM and RAM.



5. .Assembly program

```
ASSUME CS: CODE, DS: DATA
DATA SEGMENT
NUM1 DW 1234
NUM2 DW 4567
SUM DW ?
DATA ENDS
CODE SEGMENT
START: MOV AX, DATA
MOV DS,AX
MOV AX, NUM1
ADD AX, NUM2
MOV SUM, AX
INT 03H
CODE ENDS
END START
END.
```